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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,902	04/18/2001	Hui Wang	ACMR-001-02US	1040
20872	7590	07/03/2006	EXAMINER	
MORRISON & FOERSTER LLP 425 MARKET STREET SAN FRANCISCO, CA 94105-2482			LEADER, WILLIAM T	
			ART UNIT	PAPER NUMBER

1742

DATE MAILED: 07/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/837,902	Applicant(s) WANG, HUI	
	Examiner William T. Leader	Art Unit 1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 April 2006.
 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 110-159 is/are pending in the application.
 4a) Of the above claim(s) 111-115, 120-138, 140-142 and 149-156 is/are withdrawn from consideration.
 5) ☐ Claim(s) _____ is/are allowed.
 6) ☒ Claim(s) 110, 116-119, 139, 143-148 and 157-159 is/are rejected.
 7) ☐ Claim(s) _____ is/are objected to.
 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some * c) ☐ None of:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Receipt of the papers filed on April 17, 2006, is acknowledged. Claims 110-159 are pending. Applicant has identified claims 110, 116-119, 139, 143-148 and 157-159 as reading on the elected species. Claims 111-115, 120-138, 140-142 and 149-156 remain withdrawn from consideration.
2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
3. Claims 110, 116-119, 139, 143-148 and 157-159 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese patent publication 4-311591 for the reasons given in the previous office action and in view of the following comments.
4. Applicant's Remarks have been considered but are not deemed to be persuasive. Applicant questions how it is possible to a) plate the entire surface of the wafer at one time, b) achieve precisely uniform film thickness, and c) have different portions reaching different thicknesses at different times during the process. Applicant apparently reads Hirohiko as requiring that all portions of the wafer be plated at exactly the same rate so that they have exactly the same thickness at each instant in the plating process.
5. Applicant's reading fails to take into account the mechanism by which metal is deposited onto a wafer in a process such as that of Hirohiko. In a semiconductor electroplating process the

resistance of the metal on the surface changes as the deposition proceeds, resulting in a variation of the current distribution. This variation of the current distribution as the process is carried out is explained as follows. Hirohiko is directed to electrodeposition onto a wafer, which conventionally is made of a semiconductor material having insufficient conductivity to allow electroplating directly onto the wafer itself. In electroplating metals onto a wafer, a conductive seed layer is typically first deposited on the wafer to facilitate electrodeposition of the metal. The seed layer is needed to overcome the low conductivity of the wafer itself because the wafer serves as the cathode of the electroplating cell, which requires that the wafer surface be conductive. However, because the seed layer is initially very thin, the seed layer has a significant resistance radially from the edge to the center of the wafer. This resistance contributes to a potential drop from the edge where contact is made to the center of the wafer. (As shown in figure 3 and 4 of Hirohiko, wafer 9 is contacted by electrically conductive layer 32 at its peripheral edge.) Thus, the potential of the seed layer is initially not uniform, being more negative at the edge of the wafer. Consequently, the initial electrodeposition rate tends to be greater at the edge of the wafer relative to the interior of the wafer. As the thickness of the metal deposit grows, the conductivity of the wafer increases and the potential across the wafer becomes more uniform so that the current distribution across the wafer becomes more uniform. Deposition becomes more uniform radially across the wafer. Thus, even though ultimate objective of Hirohiko is to produce a precisely uniform deposit, nonuniformities occur during the course of the deposition process. See, for example, the discussion of "terminal effect" at column 1, lines 32-61 of Broadbent (6,027,631).

6. In reading applicant's claim, it is noted that it is written using the open term comprising which allows steps other than those recited to be performed. It is additionally noted that in reading process claims, it is not assumed that the process steps are performed in the order in which they are written unless the claim so specifies. As stated in the previous office action, the claim is considered to permit plating to occur simultaneously on both the first and second portions. The last step of applicant's claim 110 recites plating the film to the desired thickness on at least a second portion of the substrate surface after plating the film on the first portion of the substrate surface. Since this step recites plating the film on the first portion of the substrate surface but does not specify that the thickness on the first portion is the desired thickness, this step is read as allowing the second portion of the substrate to reach the desired thickness at any time after some deposition has occurred on the first portion. Thus, the second portion may reach the desired thickness at the same time the first portion reaches the desired thickness. The penultimate step recites plating the film to the desired thickness on a first portion of the substrate surface. This step is achieved in processes in which the first and second portions reach the desired thickness at the same time.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Japanese patent 59-150094 discloses a process and apparatus for plating a metal layer onto a disk-shaped workpiece. As in the Hirohiko patent, the objective is to plate a uniform layer. The '094 patent discloses the use of multiple independently controlled anodes. It is

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recognized that during the process plating occurs nonuniformly and that the ratio of currents to the anodes is adjusted to compensate. See page 15, lines 1-13.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William T. Leader whose telephone number is 571-272-1245. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King, can be reached on 571-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WL

William Leader
June 22, 2006

ROY KING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700